REMARKS

Examiner F. Erdem is thanked for the thorough examination and search of the subject Patent Application. Claims 17, 22, and 26 have been amended. Claims 19 and 25 have been newly canceled. Claims 1-16 remain canceled.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 17-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (U.S. 6,235,600) in view of Ding et al (U.S. 6,153,472) further in view of Krivokapic (U.S. 5,559,357) further in view of Lee et al (U.S. 6,033,981) is requested based on Amended Claim 17, Canceled Claim 19, and on the following remarks.

As has been noted, Chiang differs from Applicant's teaching in an important way. Referring to Fig. 5 of Chiang et al, the final form of the device has nitride sidewall spacers 6 but does not have a liner oxide layer overlying the polysilicon trace 3. All of the oxide layers 4, 6, 9 have been removed for the top surface of the gate 3. By comparison, Applicant Claimed invention, as shown in Figs. 7-9, has a liner oxide layer 50

overlying the polysilicon trace 56. More importantly, **Chiang et al explicitly teaches away from Applicant's Claimed invention by teaching the removal of the oxide layer 4 and the TEOS layer 6 from the top of the polysilicon line 3** as shown by the following quotation:

"An overetch cycle, for the definition of the composite insulator spacers result in the removal of the exposed region of TEOS liner 6, and of silicon oxide layer 4. (Chiang et al, Fig. 5, Col. 4, lines 15-18)".

Because Chiang et al teaches away from a key feature of the Applicant's claimed invention, Applicant respectfully submits it is cannot be obvious to one skilled in the art at the time of the invention to combine the secondary art references of Ding et al, Krivokapic, or Lee et al with Chiang et al to derive Applicant's claimed invention. Rather, any combination of Chaing et al with the secondary references would result in something other than Applicant's claimed invention since Chaing et al expressly teaches away from this key feature and since none of the cited secondary art provides a motivation to overcome this teaching away in Chiang et al.

To make clear the distinctiveness of Applicant's claimed invention, Applicant has amended Claim 17 as follows:

17. (Currently Amended) A MOSFET device comprising:

a gate comprising a polysilicon trace overlying a semiconductor substrate with an insulator therebetween;

a source region and a drain region in said semiconductor substrate with said polysilicon trace laterally between said source and drain regions;

~~an insulator layer overlying a semiconductor substrate;~~

~~polysilicon traces overlying said insulator layer;~~

a liner oxide layer overlying said polysilicon trace ~~traces~~ wherein said liner oxide layer covers sidewalls of said polysilicon trace ~~traces on edges where~~ at said source and drain regions ~~are planned~~ and wherein said liner oxide layer covers the top of said polysilicon trace; and

silicon nitride spacers wherein said liner oxide layer is laterally between said silicon nitride spacers and said polysilicon trace at said source and drain regions ~~on sidewalls of said polysilicon traces and overlying said liner oxide layer~~ and wherein said silicon nitride spacer have an L-shaped profile.~~; and~~

~~an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.~~

Amended Claim 17 makes clear several distinct features of the Claimed invention. In particular, Amended Claim 17 makes clear that (1) the liner oxide layer covers the top of the polysilicon trace, (2) the liner oxide layer on the sidewalls of the polysilicon trace is between the silicon nitride spacer and the polysilicon trace, (3) the spacers are on the polysilicon trace sidewalls where the source and drain regions are formed, and (4) the silicon nitride spacers have L-shaped profiles.

Regarding Chiang et al: Chiang et al does not teach the key feature of (1) the liner oxide layer covers the top of the polysilicon trace and, in fact teaches against this key feature.

Regarding Ding et al: Ding et al does not teach the key features of (2) the liner oxide layer on the sidewalls of the polysilicon trace is between the silicon nitride spacer and the polysilicon trace, (3) the spacers are on the polysilicon trace sidewalls where the source and drain regions are formed, and (4) the silicon nitride spacers have L-shaped profiles. Applicant finds that Ding et al do show a dielectric layer 114 formed

overlying the polysilicon layer 104a in Fig. 2H. However, Fig. 2H shows the device cross section across the channel from isolation 110 to isolation 110. Fig. 3 of Ding et al shows the cross section along the transistor ON current direction (or the direction that would show the source/drain regions in subsequent process steps). Fig. 3 of Ding et al corresponds, therefore, to the cross section depicted by the Applicant in Figs. 3 through 8. Note in Fig. 3 of Ding et al that the dielectric layer 114 (comprising, for example ONO), overlies the polysilicon layer 104b used for the floating gate by does not cover the sidewall of this gate 104b at the edges where source/drain regions would be formed.

More particularly, Ding et al teach in Column 4, lines 2-13: "The polysilicon layer 116 is patterned to form a control gate structure with a strip structure as can be seen in Fig. 1 with a shaded strip region, which is about vertically across the active area 109. The patterning process with same pattern mask is continuously performed to at least pattern the dielectric layer 114, the polysilicon spacer 112a, and the polysilicon layer 104a to expose the tunneling oxide layer 102a. The polysilicon layer 104a becomes polysilicon 104b. This patterning effect can be seen in another cross section view. Fig. 3 is a cross-sectional view of a portion of the substrate taken allon a

line II-II in Fig. 1, schematically illustrating the structure of the flash memory, according to the preferred embodiment of the invention."

From the above citation, it is seen that Ding et al teach away from leaving this dielectric layer 114 covering the sidewalls of the polysilicon trace on the source/drain edges. By comparison, Applicant's claimed invention specifically teaches the combined features of the liner oxide element, namely, that it overlies the polysilicon trace and that it covers the sidewalls of the trace at the edges where the source and drain regions will be formed.

Regarding Krivokapic: Krivokapic does not teach the key features of (1) the liner oxide layer covers the top of the polysilicon trace, (2) the liner oxide layer on the sidewalls of the polysilicon trace is between the silicon nitride spacer and the polysilicon trace, and (4) the silicon nitride spacers have L-shaped profiles. Referring to Fig. 10 of Krivokapic, silicon nitride spacers 36 are formed on the sidewalls of the polysilicon trace 44. However, there is no liner oxide layer between the nitride spacers 36 and the polysilicon trace 44. Rather, the oxide liner 36 is formed on the outside edges of the nitride spacers 36. In addition, the silicon nitride spacers 36

do not have an L-shaped profile. Finally, there is no liner oxide layer overlying the polysilicon trace 44. Rather, a polysilicon plug 50g is formed overlying the polysilicon trace 44.

Regarding Lee et al: Lee et al does not teach the key features of (1) the liner oxide layer covers the top of the polysilicon trace, (2) the liner oxide layer on the sidewalls of the polysilicon trace is between the silicon nitride spacer and the polysilicon trace, and (4) the silicon nitride spacers have L-shaped profiles. Referring now to Fig. 9, the silicon nitride spacers 20 are formed on the sidewalls of the polysilicon traces 12. However, there is no liner oxide layer between the spacers 20 and the polysilicon traces 12 or overlying the polysilicon traces 12. In addition, the spacers 12 bear a standard profile and not the L-shaped profile of the Claimed invention.

As can be seen from the above analysis, Chiang et al, Ding et al, Krivokapic, and Lee et al do not teach or suggest, separately or in combination, all of the features of the claimed invention as recited by Amended Claim 17. Further, Chiang et al teaches away from a key feature ((1) liner oxide layer overlying the polysilicon trace) of the claimed invention. Of the cited secondary art Krivokapic and Lee et al do not teach this key

feature and so could not be combined with Chiang et al to produce the claimed invention, even if there were motivation to overcome the teaching away found in Chiang et al. Even if Ding et al were construed to teach the key feature of (1) liner oxide layer overlying the polysilicon trace, there is found no motivation in Ding et al to overcome the clear teaching away found in Chiang et al.

Applicant therefore respectfully submits that it is not obvious, for one skilled in the art at the time of the invention, to combine the teachings of Chiang et al and Ding et al, Krivokapic, and/or Lee et al to derive Applicant's Claimed invention, as recited in Amended Claim 17. Further, Applicant respectfully requests that the rejection of Claim 17, under 35 U.S.C. 103(a) be removed due to reasons stated above. Further, Claims 18 and 20-21 represent patentably distinct, further limitations on Amended Claim 17 and should not be rejected under 35 U.S.C. 103(a) if Amended Claim 17 is not rejected under 35 U.S.C. 103(a). Claim 19 has been canceled as redundant in light of Amended Claim 17.

Reconsideration of Claims 17-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (U.S. 6,235,600) in view of Ding et al (U.S. 6,153,472) further in view of

Krivokapic (U.S. 5,559,357) further in view of Lee et al (U.S. 6,033,981) is requested based on Amended Claim 17, Canceled Claim 19, and on the above remarks.

Reconsideration of Claims 22-25 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (U.S. 6,235,600) in view of Ding et al (U.S. 6,153,472) further in view of Chen et al (U.S. 6,323,105) further in view of Krivokapic (U.S. 5,559,357) further in view of Thomas (U.S. 6,590,265) is requested based on Amended Claim 22, Canceled Claim 25, and on the following remarks.

Applicant references the analysis above regarding the rejection of Claims 17-21 under 35 U.S.C. 103(a). Claim 22 has been amended in similar fashion to Amended Claim 17. Amended Claim 22 now reads:

22. (Currently Amended) A MOSFET device comprising:

a gate comprising a polysilicon trace overlying a semiconductor substrate with an insulator therebetween;

a source region and a drain region in said semiconductor substrate with said polysilicon trace laterally between said source and drain regions;

~~an insulator layer overlying a semiconductor substrate;~~

~~polysilicon traces overlying said insulator layer wherein said polysilicon traces comprise transistor gates;~~

a liner oxide layer overlying said polysilicon trace ~~traces~~ wherein said liner oxide layer covers sidewalls of said polysilicon trace ~~traces on edges where~~ at said source and drain regions ~~are planned~~ and wherein said liner oxide layer covers the top of said polysilicon trace; and

silicon nitride spacers wherein said liner oxide layer is laterally between said silicon nitride spacers and said polysilicon trace at said source and drain regions, ~~on sidewalls of said polysilicon traces and overlying said liner oxide layer~~ wherein said silicon nitride spacers have an L-shaped profile, and wherein said silicon nitride layer is formed by one of the group of: growing by thermal process.~~; and~~

~~an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.~~

Therefore, Amended Claim 22 also recites the same key features of (1) the liner oxide layer covers the top of the polysilicon trace, (2) the liner oxide layer on the sidewalls of the

polysilicon trace is between the silicon nitride spacer and the polysilicon trace, (3) the spacers are on the polysilicon trace sidewalls where the source and drain regions are formed, and (4) the silicon nitride spacers have L-shaped profiles.

Regarding Chiang et al, Ding et al, and Krivokapic, Applicant references the analysis shown above for Claims 17-21.

Regarding Thomas: Thomas does not teach the key features of (1) the liner oxide layer covers the top of the polysilicon trace and (4) the silicon nitride spacers have L-shaped profiles. Referring to Fig. 3B of Thomas, the cross section shows spacers 810 and 720. However, there is no liner oxide layer overlying the polysilicon trace 840. In addition, the spacer profiles are rotated 180° from those shown in Applicant's claimed invention.

As can be seen from the above analysis, Chiang et al, Ding et al, Krivokapic, and Thomas do not teach or suggest, separately or in combination, all of the features of the claimed invention as recited by Amended Claim 22. Further, Chiang et al teaches away from a key feature ((1) liner oxide layer overlying the polysilicon trace) of the claimed invention. Of the cited secondary art Krivokapic and Thomas do not teach this key

feature and so could not be combined with Chiang et al to produce the claimed invention, even if there were motivation to overcome the teaching away found in Chiang et al. Even if Ding et al were construed to teach the key feature of (1) liner oxide layer overlying the polysilicon trace, there is found no motivation in Ding et al to overcome the clear teaching away found in Chiang et al.

Applicant therefore respectfully submits that it is not obvious, for one skilled in the art at the time of the invention, to combine the teachings of Chiang et al and Ding et al, Krivokapic, and/or Thomas to derive Applicant's Claimed invention, as recited in Amended Claim 22. Further, Applicant respectfully requests that the rejection of Claim 22, under 35 U.S.C. 103(a) be removed due to reasons stated above. Further, Claims 23-24 represent patentably distinct, further limitations on Amended Claim 22 and should not be rejected under 35 U.S.C. 103(a) if Amended Claim 22 is not rejected under 35 U.S.C. 103(a). Claim 25 has been canceled as redundant in light of Amended Claim 22.

Reconsideration of Claims 22-25 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (U.S. 6,235,600) in view of Ding et al (U.S. 6,153,472) further in view of Chen

et al (U.S. 6,323,105) further in view of Krivokapic (U.S. 5,559,357) further in view of Thomas (U.S. 6,590,265) is requested based on Amended Claim 22, Canceled Claim 25, and on the above remarks.

Reconsideration of Claims 26-28 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (U.S. 6,235,600) in view of Ding et al (U.S. 6,153,472) further in view of Tsai (U.S. 6,251,748) further in view of Krivokapic (U.S. 5,559,357) further in view of Thomas (U.S. 6,590,265) is requested based on Amended Claim 26 and on the following remarks.

Applicant references the analysis above regarding the rejection of Claims 17-21 under 35 U.S.C. 103(a). Claim 26 has been amended in similar fashion to Amended Claim 17. Amended Claim 26 now reads:

26. (Currently Amended) A MOSFET device comprising:

a gate comprising a polysilicon trace overlying a semiconductor substrate with an insulator therebetween;

a source region and a drain region in said semiconductor substrate with said polysilicon trace laterally between said source and drain regions;

~~an insulator layer overlying a semiconductor substrate;~~

~~polysilicon traces overlying said insulator layer wherein said polysilicon traces comprise transistor gates;~~

a liner oxide layer overlying said polysilicon trace ~~traces~~ wherein said liner oxide layer covers sidewalls of said polysilicon trace ~~traces on edges where~~ at said source and drain regions ~~are planned~~ and wherein said liner oxide layer covers the top of said polysilicon trace; and

silicon nitride spacers wherein said liner oxide layer is laterally between said silicon nitride spacers and said polysilicon trace at said source and drain regions, ~~on sidewalls of said polysilicon traces and overlying said liner oxide layer~~ wherein said silicon nitride spacers have an L-shaped profile, and wherein said silicon nitride layer is formed by chemical vapor deposition.~~; and~~

~~an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.~~

Therefore, Amended Claim 26 also recites the same key features of (1) the liner oxide layer covers the top of the polysilicon trace, (2) the liner oxide layer on the sidewalls of the polysilicon trace is between the silicon nitride spacer and the

polysilicon trace, (3) the spacers are on the polysilicon trace sidewalls where the source and drain regions are formed, and (4) the silicon nitride spacers have L-shaped profiles.

Regarding Chiang et al, Ding et al, and Krivokapic, Applicant references the analysis shown above for Claims 17-21.

Regarding Tsai: Tsai does not teach the key features of (1) the liner oxide layer covers the top of the polysilicon trace, (2) the liner oxide layer on the sidewalls of the polysilicon trace is between the silicon nitride spacer and the polysilicon trace, (3) the spacers are on the polysilicon trace sidewalls where the source and drain regions are formed, and (4) the silicon nitride spacers have L-shaped profiles. Referring to Fig. 10 of Tsai, Tsai shows a method to form a STI structure. Silicon nitride spacers 114 are formed on the sidewalls of the polysilicon traces 104. However, no liner oxide layer overlies the polysilicon traces, no liner oxide layer is between the silicon nitride spacers 114 and the polysilicon traces 104, the spacers do not have an L-shaped profile, and there are no source/drain regions for reference.

As can be seen from the above analysis, Chiang et al, Ding et al, Krivokapic, and Tsai do not teach or suggest, separately

or in combination, all of the features of the claimed invention as recited by Amended Claim 26. Further, Chiang et al teaches away from a key feature ((1) liner oxide layer overlying the polysilicon trace) of the claimed invention. Of the cited secondary art Krivokapic and Tsai do not teach this key feature and so could not be combined with Chiang et al to produce the claimed invention, even if there were motivation to overcome the teaching away found in Chiang et al. Even if Ding et al were construed to teach the key feature of (1) liner oxide layer overlying the polysilicon trace, there is found no motivation in Ding et al to overcome the clear teaching away found in Chiang et al.

Applicant therefore respectfully submits that it is not obvious, for one skilled in the art at the time of the invention, to combine the teachings of Chiang et al and Ding et al, Krivokapic, and/or Tsai to derive Applicant's Claimed invention, as recited in Amended Claim 26. Further, Applicant respectfully requests that the rejection of Claim 26, under 35 U.S.C. 103(a) be removed due to reasons stated above. Further, Claims 27-28 represent patentably distinct, further limitations on Amended Claim 26 and should not be rejected under 35 U.S.C. 103(a) if Amended Claim 26 is not rejected under 35 U.S.C. 103(a).

Reconsideration of Claims 26-28 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (U.S. 6,235,600) in view of Ding et al (U.S. 6,153,472) further in view of Tsai (U.S. 6,251,748) further in view of Krivokapic (U.S. 5,559,357) further in view of Thomas (U.S. 6,590,265) is requested based on Amended Claim 26 and on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and have discussed their impact on the present invention above.

Allowance of all Claims is requested.

It is requested that should the Examiner not find that the Claims are now Allowable that the Examiner call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

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